Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.170”**

**.170”**

**SOURCE**

**GATE**

**BACKSIDE IS DRAIN**

**Top Material: Al**

**Backside Material: Cr/Ni/Ag**

**Bond Pad Size: G = .020 x .022” min.**

**Backside Potential: Drain**

**Mask Ref: GEN V**

**APPROVED BY: DK DIE SIZE .170” X .170” DATE: 7/11/22**

**MFG: INT’L RECTIFIER THICKNESS .014” P/N: IRFC250N**

**DG 10.1.2**

#### Rev B, 7/19/02